

## Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

### **Listing of Claims**

1. **(currently amended):** A method for fabricating a semiconductor device comprising:

forming a device isolation region on a semiconductor substrate to define a cell array region and a peripheral circuit region;

forming a first gate in the cell array region, a second gate in the peripheral circuit region, and a third gate in the peripheral circuit region;

implanting first impurity ions of a low concentration into a first portion of the semiconductor substrate adjacent to the second and third gates, using the second and third gates as a mask, to form a first impurity diffusion region of a first conductivity type;

forming first gate spacers on lateral sides of the first, second, and third gates;

implanting second impurity ions of a low concentration into a second portion of the semiconductor substrate adjacent to the first gate and first gate spacers on the lateral sides of the first gate, using the first gate and first gate spacers as a mask, to form a second impurity diffusion region of a first conductivity type;

implanting third impurity ions of a low concentration into a third portion of the semiconductor substrate adjacent to the third gate and the first gate spacers on the lateral side of the third gate, using the third gate and first gate spacers as a mask, to form a third impurity diffusion region of a second conductivity type;

forming an insulating layer over the semiconductor substrate, first through third gates, and first gate spacers;

etching the insulating layer in the peripheral region to form second gate spacers adjacent to the first spacers on the lateral side of the second and third gates, respectively;

implanting fourth impurity ions of a high concentration into a fourth portion of the semiconductor substrate adjacent to the second gate and the second spacers on the lateral sides of the first spacers of the second gate, using the second gate and the first and second spacers as a mask, to form a fourth impurity diffusion region of a first conductivity type; and

implanting fifth impurity ions of a high concentration into a fifth portion of the semiconductor substrate adjacent to the third gate and the second spacers on the lateral side of the third gate, using the third gate and first and second spacers as a mask, to form a fifth impurity diffusion region of a second conductivity type.

2. **(original):** A method for fabricating a semiconductor device, as recited in claim 1, wherein the first conductivity type is n-type.

3. **(original):** A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of first impurity ions has a lower ion diffusivity than the step of implanting second impurity ions.

4. **(original):** A method for fabricating a semiconductor device, as recited in claim 1, wherein the first through third gates comprise polysilicon.

5. **(original):** A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of first impurity ions is performed using arsenic with a dose range of about  $5 \times 10^{12}$  ions/cm<sup>2</sup> and at an energy range of about 50 keV.

6. **(original):** A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of second impurity ions is performed using

phosphorous with a dose range of about  $5 \times 10^{12}$  ions/cm<sup>2</sup> and at an energy range of about 30 keV.

7. **(previously presented):** A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of third impurity ions is performed using boron with a dose range of about  $1 \times 10^{13}$  ions/cm<sup>2</sup> and at an energy range of about 20 keV.

8. **(original):** A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of fourth impurity ions is performed using arsenic with a dose range of about  $5 \times 10^{15}$  ions/cm<sup>2</sup> and at an energy range of about 50 keV.

9. **(previously presented):** A method for fabricating a semiconductor device, as recited in claim 1, wherein the implanting of fifth impurity ions is performed using boron fluoride (BF<sub>2</sub>) with a dose range of about  $5 \times 10^{15}$  ions/cm<sup>2</sup> and at an energy range of about 20 keV.

10. **(previously presented):** A method for fabricating a semiconductor device, as recited in claim 1, further comprising:

forming a silicide layer over the semiconductor substrate, the second gate, and the third gate in the peripheral circuit region; and

forming an interlayer insulating layer over the substrate and first through third gates;

etching a selected portion of the interlayer insulating layer in the cell array region, using the insulating layer as an etching stopper, and forming a contact opening adjacent to the first gate.

11. **(original):** A method for fabricating a semiconductor device, as recited in claim 10, wherein the forming of a silicide layer is further comprises

forming a transition metal over the substrate and the second and third gates  
annealing the substrate and the transition metal to form the silicide layer.

12. **(previously presented):** A method for fabricating a semiconductor device, as recited in claim 11, wherein during the annealing of the substrate and the transition metal, the first through fifth impurities are diffused into the first through fifth impurity diffusion regions, respectively.

13. **(original):** A method for fabricating a semiconductor device, as recited in claim 10, wherein the a remaining portion of the insulating layer, after the etching of the insulating layer in the peripheral region, serves as a barrier layer to prevent silicidation in the cell array area during the forming of a silicide layer.

14. **(original):** A method for fabricating a semiconductor device, as recited in claim 10, wherein the interlayer insulating layer has a first etching rate at least five times as high as a second etching rate of the insulating layer.

15. **(currently amended):** A method for fabricating ~~an MOS transistor in~~ a semiconductor device, the method comprising the steps of:

forming a first gate electrode over a PMOS region of semiconductor substrate and a second gate electrode over an NMOS region of the semiconductor substrate;

implanting first impurity ions at a low concentration of a first conductivity type, using the first and second gate electrode electrodes as a mask, to form [[a]] first impurity diffusion [[layer]] layers in the NMOS and PMOS regions;

forming first spacers on lateral sides of the first gate electrode and second spacers on lateral sides of the second gate electrode;

masking the NMOS region while implanting second impurity ions at a low concentration of a second conductivity type, using the first gate electrodes and first spacers as a mask, to form a second impurity diffusion layer in the PMOS region;

forming a ~~second~~ third spacers adjacent to the first spacers, and fourth  
spacers adjacent the second spacers;

implanting third impurity ions of high concentration of a second conductivity type, using the first and second gate electrodes and the first ~~and second~~ through fourth spacers as a mask, to form ~~[[a]]~~ third impurity diffusion ~~[[layer]]~~ layers in the PMOS and NMOS regions; and

annealing and diffusing the impurity diffusion layers to define a single  
lightly-doped drain (LDD) structure in the NMOS region and a double LDD  
structure in the PMOS region ~~overlap the first diffusion layer with the second~~  
~~diffusion layer.~~

16. **(currently amended):** A method for fabricating a ~~MOS transistor in a~~ semiconductor device, as recited in claim 15, wherein the first conductivity type is n-type and the second conductivity type is p-type.

17. **(currently amended):** A method for fabricating a ~~MOS transistor in a~~ semiconductor device, as recited in claim 15, wherein the implanting of first impurity ions is performed using arsenic with a dose range of about  $5 \times 10^{12}$  ions/cm<sup>2</sup> and at an energy range of about 50 keV.

18. **(currently amended):** A method for fabricating a ~~MOS transistor in a~~ semiconductor device, as recited in claim 15, wherein the implanting of second impurity ions is performed using boron with a dose range of about  $1 \times 10^{13}$  ions/cm<sup>2</sup> and at an energy range of about 20 keV.

19. **(currently amended):** A method for fabricating a ~~MOS transistor in a~~ semiconductor device, as recited in claim 15, wherein the implanting of third impurity ions is performed using boron fluoride (BF<sub>2</sub>) with a dose range of about  $5 \times 10^{15}$  ions/cm<sup>2</sup> and at an energy range of about 20 keV.

20. **(new):** A method of fabricating a semiconductor device, as recited in claim 15, wherein the semiconductor device includes a memory cell region and a peripheral circuit region, and the PMOS and NMOS regions are located in a peripheral circuit region.